We claim:

1) A signal processing system for a wireless communications system, said signal processing system comprising:

a baseband receiver having one or more control inputs and a status output;

a transmit modulator having a quadrature input, one or more control inputs, and a status output;

a baseband receive processor having one or more control outputs;

a baseband transmit processor having a quadrature output, a control output, and a transmit enable output;

a first multiplexer having an output, said output selecting either:

one of said baseband receive processor control outputs

or one of said baseband transmit processor quadrature outputs , said first multiplexer making a selection based on said transmit enable, said first multiplexer output coupled to a first digital to analog converter (DAC), said first DAC output coupled to one of said transmit modulator quadrature inputs and also to one of said baseband receiver control inputs;

a second multiplexer having an output, said output selecting either:

other said baseband receive processor control output or the other of said baseband transmit processor quadrature output, said second multiplexer making a selection based on said transmit enable, said second multiplexer output coupled to a second digital to analog converter (DAC), and delivering said second DAC output to the other of said transmit modulator quadrature inputs and also to the other of said baseband receiver control inputs;

a third multiplexer having an output, said output selecting either said baseband receiver status signal or said transmit modulator status signal, said third multiplexer output making a selection based on said transmit enable, said third multiplexer output coupled to a first analog to digital converter, the output of said analog to digital converter coupled to said baseband receive processor status signal and also to said baseband transmit processor status signal.

2) The signal processing system of claim 1 where said first multiplexer couples one of said baseband receive processor control signals to said first DAC when said transmit enable is not active.

3) The signal processing system of claim 2 where said baseband receive processor control signal is a gain control signal.

4) The signal processing system of claim 1 where said first multiplexer couples one of said baseband transmit processor quadrature signals to said first DAC when said transmit enable is active.

5) The signal processing system of claim 1 where said second multiplexer couples one of said baseband receive processor control signals to said second DAC when said transmit enable is not active.

6) The signal processing system of claim 5 where said baseband receive processor control signal is a gain control signal.

7) The signal processing system of claim 1 where said second multiplexer couples one of said baseband transmit processor quadrature signals to said second DAC when said transmit enable is active.

8) The signal processing system of claim 1 where said third multiplexer couples said baseband receiver status signal to said ADC when said transmit enable is not active.

9) The signal processing system of claim 8 where said baseband receiver status signal is receive signal strength indication.

10) The signal processing system of claim 1 where said third multiplexer couples said transmit modulator status signal to said third ADC when said transmit signal is active.

11) The signal processing system of claim 10 where said transmit modulator status signal is a transmit power strength.

12) The signal processing system of claim 1 where at least one of said baseband receive processor or said baseband transmit processor is a digital circuit.

13) The signal processing system of claim 12 where said digital circuit is an integrated circuit.

14) The signal processing system of claim 12 where said digital circuit is a field programmable gate array (FPGA).

15) A signal processing system for a wireless communications system, said signal processing system comprising:

a baseband receiver having one or more control inputs and a status output;

a transmit modulator having a quadrature input, one or more control inputs, and a status output;

a baseband receive processor having one or more control outputs;

a baseband transmit processor having a quadrature output, a control output, and a transmit enable output;

a first multiplexer having an output, said output selecting one of:

said baseband receive processor control output or one of said baseband transmit processor quadrature outputs, said first multiplexer making a selection based on said transmit enable, said first multiplexer output coupled to a first digital to analog converter (DAC), said first DAC output coupled to one of said transmit modulator quadrature inputs and also to one of said baseband receiver control inputs;

a second multiplexer having an output, said output selecting either:

other said baseband receive processor control output or the other of said baseband transmit processor quadrature outputs, said second multiplexer making a selection based on said transmit enable, said second multiplexer output coupled to a second digital to analog converter (DAC), and delivering said second DAC output to the other of said transmit modulator quadrature inputs and also to the other of said baseband receiver control inputs.

16) The signal processing system of claim 15 where said first multiplexer couples one of said baseband receive processor control signals to said first DAC when said transmit enable is not active.

17) The signal processing system of claim 16 where said baseband receive processor control signal is a gain control signal.

18) The signal processing system of claim 15 where said first multiplexer couples one of said baseband transmit processor quadrature signals to said first DAC when said transmit enable is active.

19) The signal processing system of claim 15 where said second multiplexer couples one of said baseband receive

processor control signals to said second DAC when said transmit enable is not active.

20) The signal processing system of claim 19 where said baseband receive processor control signal is a gain control signal.

21) The signal processing system of claim 15 where said second multiplexer couples one of said baseband transmit processor quadrature signals to said second DAC when said transmit enable is active.

22) The signal processing system of claim 1 or 15 where said baseband receiver quadrature outputs and said transmit modulator quadrature input signals are analog signals.

23) The signal processing system of claim 1 or 15 where said baseband receive processor quadrature inputs and said baseband transmit processor outputs are digital signals having more than one bit of width.

24) A signal processing system for a wireless communications system, said signal processing system comprising:

a baseband receiver having one or more control inputs, quadrature outputs, and a status output;

a transmit modulator having a quadrature input, one or more control inputs, and a status output;

a baseband receive processor having one or more control outputs, a multiplexer control, and a quadrature input;

a baseband transmit processor having a quadrature output, a sample output, and a transmit enable output;

a first multiplexer having an output which selects between one of:

said baseband receive processor control outputs or one of said baseband transmit processor quadrature outputs in response to said transmit enable, said first multiplexer output coupled to a first digital to analog converter (DAC), and delivering said first DAC output to one of said transmit modulator quadrature inputs and also to one of said baseband receiver control inputs;

a sample and hold having an input coupled to said first DAC output and an output coupled to one of said transmit modulator control signals, said sample and hold controlled by said baseband transmit processor said sample output;

a second multiplexer having an output, said second multiplexer output coupled to one of:

other said baseband receive processor control output or the other of said baseband transmit processor quadrature

output in response to said transmit select, said second multiplexer output coupled to a second digital to analog converter (DAC) and delivering said second DAC output to the other of said transmit modulator quadrature inputs and also to the other of said baseband receiver control inputs;

a third multiplexer having an output, said third multiplexer output coupled to either of:

one of said baseband receiver quadrature outputs or said baseband receiver status signal in response to said baseband receiver processor said multiplexer control, said third multiplexer output coupled to a first analog to digital converter, the output of said analog to digital converter coupled to said baseband receive processor status signal and also to one of said baseband receiver quadrature inputs;

a fourth multiplexer having an output, said fourth multiplexer output coupled to one of:

the other said baseband receiver quadrature output or said transmit modulator status signal, said fourth multiplexer selection controlled by said baseband transmit processor said transmit enable, said fourth multiplexer output coupled to a second analog to digital converter (ADC), the output of said second ADC coupled to the other said receive processor quadrature input and said baseband transmit processor status signal.

25) The signal processing system of claim 24 where said first multiplexer couples one of said baseband receive processor control signals to said first DAC when said transmit enable is not active.

26) The signal processing system of claim 25 where said baseband receive processor control signal is a gain control signal.

27) The signal processing system of claim 24 where said first multiplexer couples one of said baseband transmit processor quadrature signals to said first DAC when said transmit enable is active.

28) The signal processing system of claim 24 where said second multiplexer couples one of said baseband receive processor control signals to said second DAC when said transmit enable is not active.

29) The signal processing system of claim 28 where said baseband receive processor control signal is a gain control signal.

30) The signal processing system of claim 24 where said second multiplexer couples one of said baseband transmit processor quadrature signals to said second DAC when said transmit enable is active.

31) The signal processing system of claim 24 where said third multiplexer couples said baseband receiver status signal to said ADC when said receive processor said multiplexer control is not active.

32) The signal processing system of claim 31 where said baseband receiver status signal is receive signal strength indication.

33) The signal processing system of claim 24 where said third multiplexer couples one of said baseband receiver quadrature outputs to said first ADC when said receiver processor said multiplexer control is active.

34) The signal processing system of claim 24 where a transmit gain value is placed on one of said baseband transmit processor quadrature outputs and said sample output is active.

35) The signal processing system of claim 24 where at least one of said baseband receive processor or said baseband transmit processor is a digital circuit.

36) The signal processing system of claim 35 where said digital circuit is an integrated circuit.

37) The signal processing system of claim 35 where said digital circuit is a field programmable gate array (FPGA).

38) The signal processing system of claim 1 where said first multiplexer includes a test input which is coupled to said first DAC or to said DAC, selectable by said transmit enable.

39) The signal processing system of claim 1 where said second multiplexer includes a test input which is coupled to said first DAC or to said second DAC, selectable by said transmit enable.

40) The signal processing system of claim 15 where said first multiplexer includes a test input which is coupled to said first DAC or to said DAC, selectable by said transmit enable.

41) The signal processing system of claim 15 where said first multiplexer includes a test input which is coupled to said first DAC or to said DAC, selectable by said transmit enable.

42) The signal processing system of claim 24 where said third multiplexer includes a test input which is coupled to said first DAC or to said DAC.

43) The signal processing system of claim 24 where said fourth multiplexer includes a test input which is coupled to said first DAC or to said DAC.

ABSTRACT

A baseband receiver having quadrature analog outputs and a plurality of analog control and status signals and a transmit modulator having analog quadrature inputs and a plurality of analog control and status signals are coupled to a transmit processor having a digital output and a plurality of digital control and status signals and to a receive processor having a digital input and a plurality of digital control and status signals by multiplexing analog to digital converters and digital to analog converters such that during a receive time the converters are used for a receive purpose and during a transmit time, the converters are used for a transmit purpose.